etching a plurality of substantially parallel troughs in the epitaxial layer;

forming at least two floating gate regions along sidewall regions of the troughs and separated from the sidewall regions by a gate dielectric layer;

forming gate lines between opposing floating gate regions in the troughs; and

forming control gate regions in the troughs between opposing floating gate regions and separated therefrom by an intergate dielectric layer.

47. (New) The method of claim 46, wherein the forming of the first source/drain layer includes forming the first source/drain layer with an approximate thickness between 0.2 microns and 0.5 microns.

48. (New) The method of claim 46, wherein the forming of the thin layer of silicon dioxide includes forming the thin layer of silicon dioxide with an approximate thickness of 10 nanometers.

49. (New) A method comprising:

forming a first source/drain layer at a surface of a substrate, the first source/drain layer comprising N+ silicon formed by epitaxial growth of silicon upon the substrate;

forming a semiconductor epitaxial layer on the first source/drain layer;

forming a second source/drain layer at a surface of the epitaxial layer by ion-implantation, the second source/drain layer comprising N+ silicon and having an approximate thickness of 150 nanometers;

forming a thin layer of silicon dioxide on the second source/drain layer, the thin layer of silicon dioxide having an approximate thickness of 10 nanometers;

forming a layer of silicon nitride on the thin layer of silicon dioxide, the layer of silicon nitride having an approximate thickness of 200 nanometers;

etching a plurality of substantially parallel troughs in the epitaxial layer;

forming at least two floating gate regions along sidewall regions of the troughs and separated from the sidewall regions by a gate dielectric layer;

forming gate lines between opposing floating gate regions in the troughs; and

forming control gate regions in the troughs between opposing floating gate regions and separated therefrom by an intergate dielectric layer.

50. (New) The method of claim 49, wherein the forming of the first source/drain layer includes forming of the first source/drain layer with an approximate thickness between 0.2 microns and 0.5 microns.

51. (New) The method of claim 49, wherein the forming of the at least two floating gate regions includes forming the at least two floating gate regions along the sidewall regions of the troughs and separated from the sidewall regions by the gate dielectric layer, the gate dielectric layer having an approximate thickness between 5 nanometers and 10 nanometers.

52. (New) A method comprising:

forming a first source/drain layer at a surface of a substrate, the substrate having a semiconductor-on-insulator portion, and the first source/drain layer comprising N+ silicon formed by ion-implantation of donor dopants into the substrate;

forming a semiconductor epitaxial layer on the first source/drain layer, the semiconductor epitaxial layer comprising P- silicon and having an approximate thickness of 0.6 microns;

forming a second source/drain layer at a surface of the epitaxial layer by ion-implantation, the second source/drain layer comprising N+ silicon and having an approximate thickness of 150 nanometers;

forming a thin layer of silicon dioxide on the second source/drain layer;

forming a layer of silicon nitride on the thin layer of silicon dioxide;

etching a plurality of substantially parallel troughs in the epitaxial layer;

forming at least two floating gate regions along sidewall regions of the troughs and separated from the sidewall regions by a gate dielectric layer;

forming gate lines between opposing floating gate regions in the troughs; and

forming control gate regions in the troughs between opposing floating gate regions and separated therefrom by an intergate dielectric layer.

53. (New) The method of claim 52, wherein the method further includes forming a conductive layer in the troughs.

54. (New) The method of claim 53, wherein the method further includes:

removing a portion of the conductive layer in the troughs; and

etching a portion of the substrate underlying a portion of the troughs between the floating gate regions.

55. (New) A method comprising:

forming a first source/drain layer at a surface of a substrate, the first source/drain layer comprising N+ silicon formed by ion-implantation of donor dopants into the substrate;

forming a second source/drain layer at a surface of an epitaxial layer, the epitaxial layer being formed on the first source/drain layer and comprising P- silicon;

forming a thin layer of silicon dioxide on the second source/drain layer;

forming a layer of silicon nitride on the thin layer of silicon dioxide;

etching a plurality of substantially parallel troughs in the epitaxial layer;

forming an insulating layer undercutting semiconductor regions between the troughs;

forming at least two floating gate regions along sidewall regions of the troughs and separated from the sidewall regions by a gate dielectric layer;

forming gate lines between opposing floating gate regions in the troughs; and

forming control gate regions in the troughs between opposing floating gate regions and separated therefrom by an intergate dielectric layer.

56. (New) The method of claim 55, wherein the forming of the at least two floating gates includes forming the at least two floating gate regions along the sidewall regions of the troughs and separated from the sidewall regions by the gate dielectric layer, the gate dielectric layer having an approximate thickness between 5 nanometers and 10 nanometers.

57. (New) The method of claim 55, wherein the forming of the control gate regions includes forming of the control gate regions in the troughs between opposing floating gate regions and separated therefrom by the intergate dielectric layer, the intergate dielectric layer having an approximate thickness between 7 nanometers and 15 nanometers.

58. (New) A method comprising:

forming a first source/drain layer at a surface of a substrate;

forming a second source/drain layer at a surface of an epitaxial layer, the epitaxial layer being formed on the first source/drain layer;

etching a plurality of substantially parallel troughs in the epitaxial layer;

forming a thin silicon nitride oxidation barrier layer by chemical vapor deposition on sidewall regions of the troughs;

anisotropically etching the thin silicon nitride oxidation barrier layer to expose bottom portions of the troughs;

forming a bottom insulation layer on the bottom portions of the troughs by thermal oxidation;

forming at least two floating gate regions along sidewall regions of the troughs and separated from the sidewall regions by a gate dielectric layer; and

forming control gate regions in the troughs between opposing floating gate regions and separated therefrom by an intergate dielectric layer.

59. (New) The method of claim 58, wherein the method further includes planarizing the first conductive layer by using a chemical mechanical polish.

60. (New) The method of claim 58, wherein the method further includes stripping the thin silicon nitride oxidation barrier layer from the sidewall regions by a brief phosphoric acid etch.

61. (New) The method of claim 58, wherein the forming of the first source/drain layer includes forming the first source/drain layer at the surface of the substrate, wherein the substrate is a bulk semiconductor.

62. (New) A method comprising:

forming a first source/drain layer at a surface of a substrate;

forming a second source/drain layer at a surface of an epitaxial layer;

etching, in a first direction, a plurality of substantially parallel first troughs in the epitaxial layer;

forming first floating gate regions along sidewall regions of the first troughs and separated from the sidewall regions by a first gate dielectric layer;

forming first control gate regions between opposing first floating gate regions, the first control gate regions being separated from the first floating gate regions by a first intergate dielectric layer;

etching, in a second direction substantially orthogonal to the first direction, a plurality of substantially parallel second troughs in the epitaxial layer;

forming second floating gate regions along sidewall regions of the second troughs and separated from the sidewall regions by a second gate dielectric layer; and

forming second control gate regions between opposing second floating gate regions, the second control gate regions being separated from the second floating gate regions by a second intergate dielectric layer.

63. (New) The method of claim 62, wherein the method further includes forming a first bottom insulation layer on bottom portions of the first troughs by thermal oxidation.

64. (New) The method of claim 63, wherein the method further includes forming a second bottom insulation layer on bottom portions of the second troughs by thermal oxidation.

65. (New) The method of claim 62, wherein the method further includes forming the second intergate dielectric layer by thermal growth of silicon dioxide.

66. (New) The method of claim 62, wherein the method further includes forming the second intergate dielectric layer by deposition of oxynitride by chemical vapor deposition.

67. (New) The method of claim 62, wherein the forming of the first source/drain layer includes forming the first source/drain layer at the surface of the substrate, wherein the substrate is a bulk semiconductor.

68. (New) The method of claim 62, wherein the forming of the first floating gate regions includes forming the first floating gate regions along the sidewall regions of the first troughs and separated from the sidewall regions by the first gate dielectric layer, the first gate dielectric layer having an approximate thickness between 5 nanometers and 10 nanometers.

69. (New) The method of claim 62, wherein the forming of the second floating gate regions includes forming the second floating gate regions along the sidewall regions of the second troughs and separated from the sidewall regions by the second gate dielectric layer, the second gate dielectric layer having an approximate thickness between 5 nanometers and 10 nanometers.